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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,815	12/30/2003	Andrew S. Grover	42.p18167	9370
8791	7590	05/14/2007	EXAMINER	
BLAKELY SOKOLOFF TAYLOR & ZAFMAN			WALTER, CRAIG E	
12400 WILSHIRE BOULEVARD			ART UNIT	PAPER NUMBER
SEVENTH FLOOR			2188	
LOS ANGELES, CA 90025-1030			MAIL DATE	DELIVERY MODE
			05/14/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/749,815	GROVER, ANDREW S.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 12 April 2007.
- 2a) This action is **FINAL**.                                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-6,8-12 and 14-18 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-6,8-12,14-18 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.
 

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) Notice of Informal Patent Application
- 6) Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Status of Claims***

1. Claims 1-6, 8-12, and 14-18 are pending in the Application.

Claims 1, 8, and 14, have been amended.

Claims 7, 13, and 19 remain cancelled.

Claims 1-6, 8-12, and 14-18 are rejected.

### ***Response to Amendment***

2. Applicant's amendments and arguments filed on 12 April 2007 in response to the office action mailed on 31 January 2007 have been fully considered but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 6, 8, 9, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fortin et al., hereinafter Fortin (US PG Publication 2004/0003223 A1,

in view of Douglis et al., hereinafter Douglis (US Patent 5,481,733) and in further view of Applicant's admitted prior art.

As for claims 1, 8 and 14, Fortin teaches a system comprising of:

- a processor (Fig. 2, element 120);
- a non-volatile cache coupled to the processor (Fig. 2, flash memory 200 can be located as a separate component (as shown by element 202) which is coupled to the processor via the system bus (element 121) – paragraph 0030, all lines). Also note, the flash memory (element 200) can also serve as a cache for the hard disk (paragraph 0036, lines 1-11 – Powering down of the system is decreased by storing data that is being sent to the disk for storage that the OS can not control such as an application writing to the disk to the flash memory for storage, hence reducing the number writes to the disk) – In other words, the flash is used as a cache by the system to reduce the access burden of the hard disk; and
- a machine readable medium having stored thereon a set of instructions (the system memory as illustrated in Fig. 2, element 130, contains RAM and ROM sections which contain the OS, application programs, boot code, etc. which are used by the system to execute all system functions).

Though Fortin teaches storing configuration data in the non-volatile memory, he fails to defining a predetermined event, the occurrence of which causes a spin-down of

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a hard disk, detecting the occurrence of the event and in response to the event, spinning down the disk and storing historical hard disk performance data.

Douglis teaches a method for managing the power distributed to a disk drive in a laptop computer, wherein a state table is stored in a memory, the memory being used to store performance data of the hard disk drive. Based upon a history of disk accesses by a user, the number of transitions between each pair of states is counted and stored in memory. The information is used to predict a future period of inactivity in order to conserve power to the disk drive (see abstract).

Douglis further teaches the historical hard disk performance data as consisting of data identifying events the produced a spin-down of the hard disk and a period of time thereafter before the hard disk was spun up. Douglis teaches spinning down a hard disk drive when it is unlikely to be accessed in the near future (col. 8, lines 15-25). A prediction is made based on the past history of disk activity, which is stored in the memory. If the most likely time for the disk to be accessed is greater than a preset threshold, then the disk is spun down (col. 8, lines 38-50). In the case of this power down, historical data is recorded (i.e. period of inactivity) which indicates that the power down occurred because the inactivity data stored indicates the threshold has been exceeded. The method Douglis teaches includes quantizing the periods of inactivity into states, therefore periods of activity, and inactivity can be recorded to more efficiently power down the system (col. 8, lines 52-63). The states that are recorded to include predicting when to spin the drive back up based on the predicated next access

(col. 10, lines 46-59). In other words, the system works to anticipate how long the drive should stay powered down before its spun back up based on the historical data.

Additionally, neither Douglis nor Fortin either, alone or in combination, teach storing data identifying the predetermined event as a cause of a spin-down of the hard disk as recited by Applicant in these claims.

This limitation however fails to render the claims patentable distinct, as storing historical hard disk data about event that result in spinning down of a hard disk is prior art, based on Applicant's own admission in the background of the original specification (see paragraph 0004, all lines). Pursuant to MPEP § 2129, “[w]here the specification identifies work done by another as “prior art”, the subject matter so identified is treated as admitted prior art.”

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin to further include Douglis's method of saving historical performance data into the cache memory of his own system used to store configuration data. By doing so, Fortin would benefit by having a means of storing the historical data of his hard disk, in order to spin down the hard drive during predicted periods of inactivity, hence conserving power of his computer system as taught by Douglis (col. 8, lines 15-25). Note, though Douglis's teaches his system as being applied to a laptop computer, it is well known to one of ordinary skill in the art that power conservation is valuable to many different computing systems, not just to a laptop computer environment.

It would have been obvious to one or ordinary skill in the art at the time of the invention for Fortin to include storing the cause of spinning down a hard disk into his

own system used to store configuration data. By doing so, Fortin could benefit from an improved power management policy capable of not only recording when a drive is powered down, but also its cause.

As for claims 2, 9 and 15, Fortin teaches the non-volatile cache as being a cache for the hard disk (the flash memory (element 200) can serve as a cache for the hard disk (paragraph 0036, lines 1-11 – Powering down of the system is decreased by storing data that is being sent to the disk for storage that the OS can not control such as an application writing to the disk to the flash memory for storage, hence reducing the number writes to the disk) – In other words, the flash is used as a cache by the system to reduce the access burden of the hard disk).

As for claim 6, Douglis teaches using the historical hard disk performance data to implement a power management policy of the hard disk (the predicated period based on historical accesses by the user ultimately leads to spinning down the disk in order to put it in low power mode (see abstract)).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin to further include Douglis's method of saving historical performance data into the cache memory of his own system used to store configuration data. By doing so, Fortin would benefit by having a means of storing the historical data of his hard disk, in order to spin down the hard drive during predicted periods of inactivity, hence conserving power of his computer system as taught by Douglis (col. 8, lines 15-25).

4. Claims 5, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fortin, Douglis and Applicant's admitted prior art as applied to claims 1, 8 and 14 above, and in further view of Sanada et al., hereinafter Sanada (US PG Publication 2001/0002173 A1).

As for claims 5, 12, and 18, though the combined teachings of Fortin, Douglis and Applicant's admitted prior art meet all the limitations of the base claims, they fail to further include the non-volatile memory consisting of a thin film electronic memory.

Sanada however teaches a semiconductor storage device and production method thereof wherein he specifically teaches manufacturing a flash memory via thin film processing techniques (paragraph 0071, all lines).

It would have been obvious to one of ordinary skill in the art at the time for Fortin in view of Douglis and in further view of Applicant's admitted prior art to include his cache memory as consisting of thin film in order to have a more optimized memory that is capable of uniform data erase in a group of memory cells with a reduced number of cell in which the data erase is excessively performed as taught by Sanada (paragraph 0039, all lines).

5. Claims 3-4, 10-11 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fortin, Douglis and Applicant's admitted prior art as applied to claims 1, 8 and 14 above, and in further view of Chou et al., hereinafter Chou (US PG Publication 2005/0055481 A1).

As for claims 3-4, 10-11 and 16-17, though the combined teachings of Fortin, Douglis and Applicant's admitted prior art meet all the limitations of the base claims,

they fail to further teach the memory include a form factor of a Mini Peripheral Component Interconnect Express (mini-PCI express) card, and interface. It is worthy to note Fortin does discuss his flash memory as a separate component such as a PC slot card, just not implemented as a mini-PCI express – see paragraph 0017, lines 1-9.

Chou however teaches a Flash drive/reader with serial-port controller and flash-memory controller mastering a second RAM-buffer bus parallel to a CPU bus. In his disclosure, Chou teaches connecting a system CPU to flash-controller, which accesses an attached flash memory, which is further connected to serial engine (see Fig. 4). This connection can be implemented in part by a mini-PCI Express (paragraph 0055, all lines). Also note, a Mini-PCI express card, must inherently posses a Peripheral Component Interconnect Express interface in order to function (i.e. communicate with the system).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin in view of Douglis and in further view of Applicant's admitted prior art to further include a mini- PCI Express in order to increasing data throughput via the buffering and a second data bus as taught by Chou (paragraph 0024, all lines).

6. Claims 1, 2, 6, 8, 9, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fortin (US PG Publication 2004/0003223 A1), in view of Douglis (US Patent 5,481,733) and in further view of Miyano (US PG Publication 2005/0219733 A1).

As for claims 1, 8 and 14, Fortin teaches a system comprising of:  
a processor (Fig. 2, element 120);

a non-volatile cache coupled to the processor (Fig. 2, flash memory 200 can be located as a separate component (as shown by element 202) which is coupled to the processor via the system bus (element 121) – paragraph 0030, all lines). Also note, the flash memory (element 200) can also serve as a cache for the hard disk (paragraph 0036, lines 1-11 – Powering down of the system is decreased by storing data that is being sent to the disk for storage that the OS can not control such as an application writing to the disk to the flash memory for storage, hence reducing the number writes to the disk) – In other words, the flash is used as a cache by the system to reduce the access burden of the hard disk; and

a machine readable medium having stored thereon a set of instructions (the system memory as illustrated in Fig. 2, element 130, contains RAM and ROM sections which contain the OS, application programs, boot code, etc. which are used by the system to execute all system functions).

Though Fortin teaches storing configuration data in the non-volatile memory, he fails to defining a predetermined event, the occurrence of which causes a spin-down of a hard disk, detecting the occurrence of the event and in response to the event, spinning down the disk and storing historical hard disk performance data.

Douglis teaches a method for managing the power distributed to a disk drive in a laptop computer, wherein a state table is stored in a memory, the memory being used to

store performance data of the hard disk drive. Based upon a history of disk accesses by a user, the number of transitions between each pair of states is counted and stored in memory. The information is used to predict a future period of inactivity in order to conserve power to the disk drive (see abstract).

Douglis further teaches the historical hard disk performance data as consisting of data identifying events that produced a spin-down of the hard disk and a period of time thereafter before the hard disk was spun up. Douglis teaches spinning down a hard disk drive when it is unlikely to be accessed in the near future (col. 8, lines 15-25). A prediction is made based on the past history of disk activity, which is stored in the memory. If the most likely time for the disk to be accessed is greater than a preset threshold, then the disk is spun down (col. 8, lines 38-50). In the case of this power down, historical data is recorded (i.e. period of inactivity) which indicates that the power down occurred because the inactivity data stored indicates the threshold has been exceeded. The method Douglis teaches includes quantizing the periods of inactivity into states, therefore periods of activity, and inactivity can be recorded to more efficiently power down the system (col. 8, lines 52-63). The states that are recorded to include predicting when to spin the drive back up based on the predicated next access (col. 10, lines 46-59). In other words, the system works to anticipate how long the drive should stay powered down before its spun back up based on the historical data.

Additionally, neither Douglis nor Fortin either, alone or in combination, teach storing data identifying the predetermined event as a cause of a spin-down of the hard disk as recited by Applicant in these claims.

Miyano however teaches a recording medium device, which maintains a log of data, which is used to determine why (i.e. cause) a particular drive powered down (i.e. failed) – paragraph 0160 all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin to further include Douglis's method of saving historical performance data into the cache memory of his own system used to store configuration data. By doing so, Fortin would benefit by having a means of storing the historical data of his hard disk, in order to spin down the hard drive during predicted periods of inactivity, hence conserving power of his computer system as taught by Douglis (col. 8, lines 15-25). Note, though Douglis's teaches his system as being applied to a laptop computer, it is well known to one of ordinary skill in the art that power conservation is valuable to many different computing systems, not just to a laptop computer environment.

It would have been obvious to one or ordinary skill in the art at the time of the invention for Fortin to include Miyano's recording medium device into his own system used to store configuration data. By doing so, Fortin could benefit by exploiting the advantages of self-diagnosing a hard drive failure without the aid of a skilled worker as described by Miyano in paragraph 0002, all lines.

Claims 2, 6, 9 and 15 are rejected based on the claim mapping and motivation as set forth in paragraph 0006, *supra*.

7. Claims 5, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fortin (US PG Publication 2004/0003223 A1), Douglis (US Patent 5,481,733) and Miyano (US PG Publication 2005/0219733 A1) as applied to

claims 1, 8 and 14 above, and in further view of Sanada et al., hereinafter Sanada (US PG Publication 2001/0002173 A1).

Claims 5, 12 and 18 are rejected based on the claim mapping as set forth in paragraph 0007, *supra*.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin in view of Douglis, in further view of Miyano to include his cache memory as consisting of thin film. By doing so, they would benefit by having a more optimized memory that is capable of uniform data erase in a group of memory cells with a reduced number of cell in which the data erase is excessively performed as taught by Sanada (paragraph 0039, all lines).

8. Claims 3-4, 10-11 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Fortin (US PG Publication 2004/0003223 A1), Douglis (US Patent 5,481,733) and Miyano (US PG Publication 2005/0219733 A1) as applied to claims 1, 8 and 14 above, and in further view of Chou et al., hereinafter Chou (US PG Publication 2005/0055481 A1).

Claims 3-4, 10-11 and 16-17 are rejected based on the claim mapping as set forth in paragraph 0008, *supra*.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Fortin, Douglis and Miyano to include a mini-PCI Express in order to increase data throughput via the buffering and a second data bus as taught by Chou (paragraph 0024, all lines).

***Response to Arguments***

9. As for the rejections under 35 U.S.C 112(2), Applicant's amendments overcome the previously set forth rejections.
10. As for the rejections under 35 U.S.C. 101, by amending paragraph 0021 of the original specification, Applicant has disclaimed "electrical, optical, acoustical and other forms of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc" from encompassing the scope of the machine readable medium as recited in claims 8-12. In light of this amendment, Examiner holds claims 8-12 statutory, since the recitation of "a machine readable medium" in claims 8-12 is limited in scope to the remaining examples listed in paragraph 0021, including "discrete hardware components as large-scale integrated circuits (LSI's), application-specific integrated circuits (ASIC's), firmware such as electrically erasable programmable read-only memory (EEPROM's)".

As for the rejections under 35 U.S.C § 103, Applicant contends (under the heading "35 U.S.C. § 103(a) Rejection over Fortin and Douglis"), "the Office Action itself takes the position that Fortin and Douglis, both alone and in combination, fail to teach or suggest at least one limitation of the claims." Applicant concludes that the claims are therefore non-obvious over Fortin and Douglis based on this alleged concession by Examiner.

This argument however is not persuasive. Applicant's attention is directed to page 4, paragraph 006 of the previous Office action which recites that these claims are in fact rejected over Fortin in view of Douglis and in further view of **Applicant's admitted prior art**. In fact, Examiner explicitly indicates that the portions alleged by

Applicant as being conceded by Examiner as not existing in either Fortin or Douglis exist in the teachings of Applicant's admitted prior art (see page 6 of the previous Office action). "This limitation however fails to render the claims patentable distinct, as storing historical hard disk data about event that result in spinning down of a hard disk is prior art, based on Applicant's own admission in the background of the original specification (see paragraph 0004, all lines). Pursuant to MPEP § 2129, "[w]here the specification identifies work done by another as "prior art", the subject matter so identified is treated as admitted prior art."

Hence, Applicant has failed to rebut Examiner's clearly and properly established *prima facie* case of obviousness for these claims, since Applicant failed to address all previously cited sources of prior art forming the rejection (i.e. Fortin, Douglis and Applicant's admitted prior art).

As for the rejections under 35 U.S.C § 103, Applicant asserts (under the heading "35 U.S.C. § 103(a) Rejection over Fortin, Douglis and Sanada"), that Sanada fails to cure the alleged deficiencies of Fortin and Douglis, therefore these claims are non-obvious. This argument however is not persuasive, as Examiner maintains that Applicant failed to address all previously cited sources of prior art forming the rejection (i.e. Fortin, Douglis, Applicant's admitted prior art and Sanada), and it is in fact Applicant's admitted prior art that teaches the alleged deficiencies of Fortin and Douglis. A similar rebuttal argument is germane to Applicant's argument under the heading "35 U.S.C. § 103(a) Rejection over Fortin, Douglis and Chou".

As for the rejections under 35 U.S.C § 103, Applicant contends (under the heading “35 U.S.C. § 103(a) Rejection over Fortin, Douglis and Minayo [sic]”), “Douglis does not store data including data identifying the predetermined event as a cause of a spin-down of the hard disk and a period of time thereafter before the hard disk was spun up.”

This argument however is not persuasive. Examiner notes this argument is substantially similar to the one presented by Applicant in the remarks section filed on 26 May 2006. Examiner addressed these arguments in the Office action made final on 18 August 2006. In the interest of providing Applicant with a fully responsive reply to these arguments, Examiner included relevant portions of the previous “Response to Arguments” section of the Office action mailed 18 August 2006 (see pages 8-10) *infra*.

Douglis discusses spinning-down the hard disk once it is determined that the disk is unlikely to be accessed in the near future (col. 8, line 15-25). This is the “event” (i.e. disk inactivity time) that leads to the spinning-down of the disk. Douglis further teaches storing (inherently as “data”) not only previous disk inactivity, but also a preset threshold time value  $T_d$  (col. 8, lines 38-52). The previous disk inactivity and the preset threshold time value are data, which are used to identify an event (i.e. inactivity of disk access). By giving this limitation its broadest reasonable with Applicant’s specification (see MPEP § 2111), Douglis does in fact teach storing data, which identifies an event, wherein that event is the cause of spinning-down the hard disk (inactivity).

Douglis further discusses storing a value (as data) representing *each* inactive time interval (emphasis added) as it occurs, and predicting a next inactive time based on the

stored values (col. 8, lines 52-63). Note Douglis discusses storing the data for each inactive time period. In other words Douglis is not limiting inactivity to accessing, but *all* periods of inactivity, which inherently includes when the disk is spun down (it must be inactive once its spun down). By storing inactivity periods, Douglis meets the limitation of storing data "including a period of time thereafter before the hard disk was spun up". Based on Examiner's broadest reasonable interpretation consistent with Applicant's specification, this limitation does not necessarily include the entire time period of when the disk was spun down, to when it was spun back up. The limitation requires storing "a period of time thereafter (from spin down) before the hard disk was spun up". This may include storing *any* time period from when the drive was spun down, to when it was spun up, and does not necessarily include the entire time period from spin down, to spin up. The states that are used to record the predictive access time are used to anticipate when to spin the drive back up (col. 10, lines 49-59) based on previous disk activity (or conversely, in activity). In other words, Douglis teaches storing "a period of time" between those two events, which can be used to predict when to spin the drive back up.

Applicant further contends, "Douglos rather stores a quantized state which represents a range of time duration periods. In other words, Douglos stores an indication that a period of disk inactivity may be any one of a range of (plural) time duration periods." Applicant further concedes that Douglos teaches, "storing a state which presents a range of plural time duration periods" (page 13 of Remarks). These statements in fact support Examiner's position. More specifically, the claim recites, "the historical data including data... **a period of time** thereafter before the hard disk was

spun up" (emphasis added). Applicant concedes that the quantized state in fact represents some time duration period, hence Examiner has sufficiently shown that Douglis stores "a time period" as recited in these claims. Applicant further contends, "storing a state which represents a range of plural time duration periods is, at best, an abstraction of data, which fails to identify a specific single time period in said range of time duration periods." This argument is not persuasive because it is not commensurate with the scope of the claim. More specifically, the claim does not recite, "a single time period", but rather "a time period". Giving this claim limitation its broadest reasonable interpretation consistent with Applicant's specification (see MPEP § 2111), storing a range of plural time duration periods, as conceded by Applicant that Douglis in fact teaches, sufficiently reads on storing "a time period" (i.e. if a plural time durations are stored, then "a time period" in fact **must** be stored as required by the claim).

Applicant set forth similar arguments (i.e. Fortin, Douglis, and Miyano fail to teach or suggest storing data identifying the predetermined event as a cause of a spin-down of the hard disk and a period of time thereafter before the hard disk was spun up) under the headings, "35 U.S.C. § 103(a) Rejection over Fortin, Douglis Miyano and Sanada" and "35 U.S.C. § 103(a) Rejection over Fortin, Douglis Miyano and Chou". These arguments are therefore not persuasive per the rebuttal arguments presented *supra*.

Applicant's argument that any and all dependant claims are allowable for at least further limiting an allegedly allowable base claim is rendered moot in view of the arguments and rejections discussed *supra*.

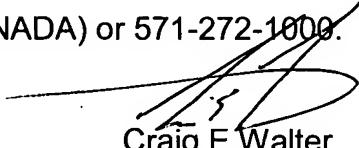
**Conclusion**

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).
12. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.
13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.
14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

  
HYUNG SOUGH  
SUPERVISORY PATENT EXAMINER

5-10-07

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Craig E Walter  
Examiner  
Art Unit 2188

CEW